**Final Report of the UGC Major Research Project**

***entitled***

**“Development of I P Core for Implementation of Image Processing Algorithms on FPGA Board”**

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**Summary of the Project**

In the area of image processing two important applications are noise filtering and image enhancement [1]. Many type of noises, including impulse noise are the normal sources of image corruption, are the subset of digital signals. Noise filtering aims to eliminate noise by affecting lesser on the original image. One of the nonlinear filters is median filter. Median filtering has proved an effective way to satisfy the dual requirements of removing impulse noise while preserving rapid signal changes. Impulse noise can appear because of a random bit error on a communication channel. This kind of noise is known as classical salt & pepper noise for grey scale image. A classic general purpose Median filter is based on a sorting approach over the entire window elements to find the median value. Median filters operate by replacing a given sample in a signal by the median of the signal values in a window around the sample. A block diagram of median filter is depicted in fig:1.

|  |  |  |
| --- | --- | --- |
| p1 | p2 | p3  Median Filter  Output |
| p4 | p5 | p6 |
| P7 | P8 | P9 |

fig.1. Block diagram of median filter

The disadvantage of median filter takes the image blur by applying it uniformly throughout that image. The pixel values of input image altered with non contaminated pixels by noise which results an overall degradation of image with distorted features.

**Hardware Architecture of Median Filter:**

Our proposed architecture follows several stages of pipelining and also parallel processing to minimize computational time. A 3x3 or 5x5 pixel neighborhood has been selected for computation of the filter output. Hardware architecture of Median filter is depicted in the fig. 2.

25 Input Lines

Median Computation

Unit

Window

Creation

Unit

Median

Output Image

Input Image

Output

Unit

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.

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fig. 2. Hardware Design of Median Filter

**Hardware Architecture of Switching Median Filter:**

Switching median filter (SMF) is used to remove the impulse noise because it cannot change or replace the noise–free pixel with median value. The algorithm’s most attractive part is its determination for which pixels filtering are needed. The switching median filter is more simple and effective than normal median filter. But the median based impulse detector fails to distinguish thin lines and impulse noise. For this reason, in case of median based filtering thin lines are removed as noise

Hardware Architecture of Switching Median Filter:

Our proposed architecture follows several stages of pipelining and also parallel processing to minimize computational time. A 3x3 or 5x5 pixel neighborhood has been selected for computation of the filter output. The hardware structure of switching median filter and the computation procedure are illustrated in fig 3.

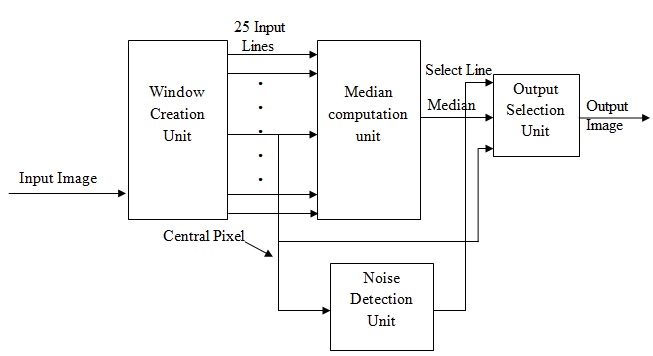


fig. 3. Hardware design of switching median filter

Table 1: Design summary of proposed Median & Switching Median Filter in terms of their Chip Utilizations

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Summary of slice Logic Utilization | Median Filter | | Switching Median Filter | |
| 3x3 | 5x5 | 3x3 | 5x5 |
| Number of Slice Registers | 1% | 1% | 1% | 1% |
| Number of Slice LUTs | 1% | 7% | 1% | 7% |
| Number used as Logic | 1% | 7% | 1% | 7% |
| Number of occupied Slices | 2% | 11% | 2% | 10% |
| Number with an unused Flip Flops | 87% | 91% | 87% | 91% |
| Number with an unused LUTs | 1% | 4% | 1% | 3% |
| Number of fully used LUTs and Flip Flop pairs | 10% | 3% | 10% | 4% |
| Number of bonded IOBs | 3% | 3% | 3% | 3% |
| Number of BUFG/BUFGCTRLs | 3% | 3% | 3% | 3% |

In fig.4, the results of the application of median filter and switching median filter are presented on 8bit grey scale “Pepper” image. More specifically, fig.4 (a), presents the original uncorrupted “pepper” image. fig.13 (b) shows the original image degraded by 5% impulse noise (salt & pepper noise). In fig. 4(c) and 4(d), the resultant images of the application of median and switching median filter for a 3x3 pixel window are shown respectively.

Table 2: Comparative results between Architecture Based Median Filter and Switching Median Filter in terms of MSE

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Peppers image | | | | Barbara image | | | |
| Size | 3x3 | | 5x5 | | 3x3 | | 5x5 | |
| Noise | 3% | 5% | 3% | 5% | 3% | 5% | 3% | 5% |
| median | 44.68 | 46.72 | 75.58 | 80.096 | 286.92 | 292.72 | 295.54 | 303.69 |
| SMF | 1.91 | 3.44 | 2.309 | 4.345 | 11.88 | 20.51 | 10.35 | 18.21 |

Table 3: Comparative results between Architecture Based Median Filter and Switching Median Filter in terms of PSNR

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Peppers image | | | | Barbara image | | | |
| Size | 3x3 | | 5x5 | | 3x3 | | 5x5 | |
| Noise | 3% | 5% | 3% | 5% | 3% | 5% | 3% | 5% |
| median | 31.62 | 31.43 | 29.35 | 29.09 | 23.55 | 23.47 | 23.42 | 23.31 |
| SMF | 45.35 | 42.76 | 44.496 | 41.75 | 37.88 | 35.01 | 37.98 | 35.53 |

**Conclusion :**

In this project, we propose the hardware implementation of switching median filter for the first time, which is highly suitable for real time imaging applications. We also present architecture based comparison of median filter and switching median filter which are capable of performing impulse noise suppression. The proposed design for SMF identifies the existence of impulse noise in the image neighborhood and applies the corresponding median computation unit only, when necessary, unlike median filter. The switching median filter avoids the blurring of the image and preserves the detail information and edge integrity compared to median filter. Table 2 and Table 3 shows the better hardware performances of switching median filter for noise removal. Chip utilization table (Table 1) shows efficient implementation and helps to understand the better hardware design of switching median filter over median filter as well. Moreover, the design of the two circuits can be easily modified to accommodate larger size windows requiring some small modifications. The proposed algorithms of the project are successfully designed and implemented on FPGA using of Genesys Virtex5 board of XC5VLX50T-2ff1136 device family.

**List of Publications :**

1.“ Identification of Red Blood Cells in Blood Cell Images using Hough Transform” Mausumi Maitra, Rahul Kr. Gupta and Manali Mukherjee Published in the proceedings of the 2nd National Conference on Computing and Systems held on 15-16 March, 2012 at the University of Burdwan (ISBN:93-80813-18-X).

2 “ Detection and Counting of Red Blood Cells in Blood Cell Images using Hough Transform” Published in the International Journal of Computer Applications (0975-8887), Vol.53-No.16, September, 2012 ,

(ISBN :973-93-80870-44-0).

3. “Studies on some speckle De-Noising Approaches in Medical Ultrasound Liver Images” by Mausumi Maitra, Manali Mukherjee and Santanu Ghosh, Published in the Proceeding of Second International Conference on Computing and Systems held on 21-22 September, 2013 at the University of Burdwan (ISBN : 10:9-35-134273—5).

4.“Comparative Study on Noise Reduction In Ultrasound Liver Images” Published in the International Journal of Computer Applications (0975 –8887), Volume 66, No.16, March, 2013 (ISBN : 973-93-80873-76-7).

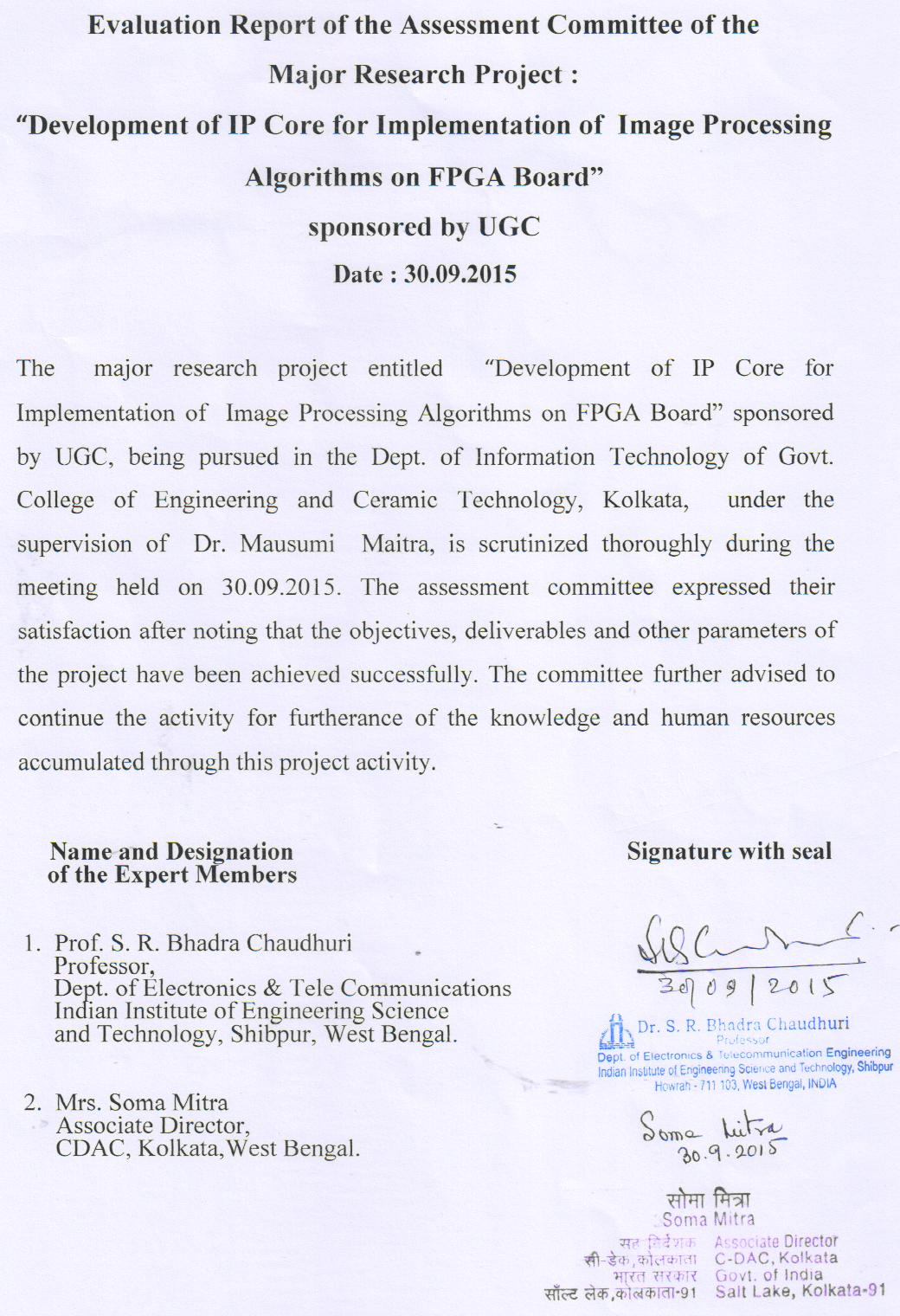
5.“Removal of Impulse Noise Using Switching Median Filter by designing its Reconfigurable Architecture” – Manali Mukherjee, Mausumi Maitra, Kamarujjaman - International Conference on Communication and Computing ICC–2014, Bangalore, June 12-14, 2014 (Elsevier Science and Technology Publication).

6. A New Decision-Based Adaptive Filter for Removal of High Density Impulse Noise from Digital Images - Kamarujjaman, Manali Mukherjee and Mausumi Maitra, ICDCCOM - 2014, September 12-13, 2014, BIT Mesra (IEEE Explorer publication)

7. An Efficient Approach for Suppression of Impulse Noise from Digital Images using Decision-Based Adaptive filter- Kamarujjaman Sk, Manali Mukherjee and Mausumi Maitra, Accepted in ICECE-14, BUET, Bangladesh, to be held during December, 2014 (not presented due to lack of fund).

8.Reconfigurable Architecture of Adaptive Median Filter – A FPGA Based Approach for Impulse Noise Suppression – Manali Mukherjee, Kamarujjaman, Mausumi Maitra was published by IEEE Xplore. Presented in 3rd International Conference on Computer, Communication, Control and Information Technology (C3IT), 2015, was held in Academy of Technology, Adisaptagram, during 7th – 8th February, 2015.

9.Kamarujjaman, Manali Mukherjee and **Mausumi Maitra,** “An efficient FPGA based de-noising architecture for removal of high density impulse noise in images”, IEEE International Conference on Research in Computational Intelligence and Communication Networks (ICRCICN), RCCIIT, Kolkata, Sept., 2015.

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